INTRODUCTION

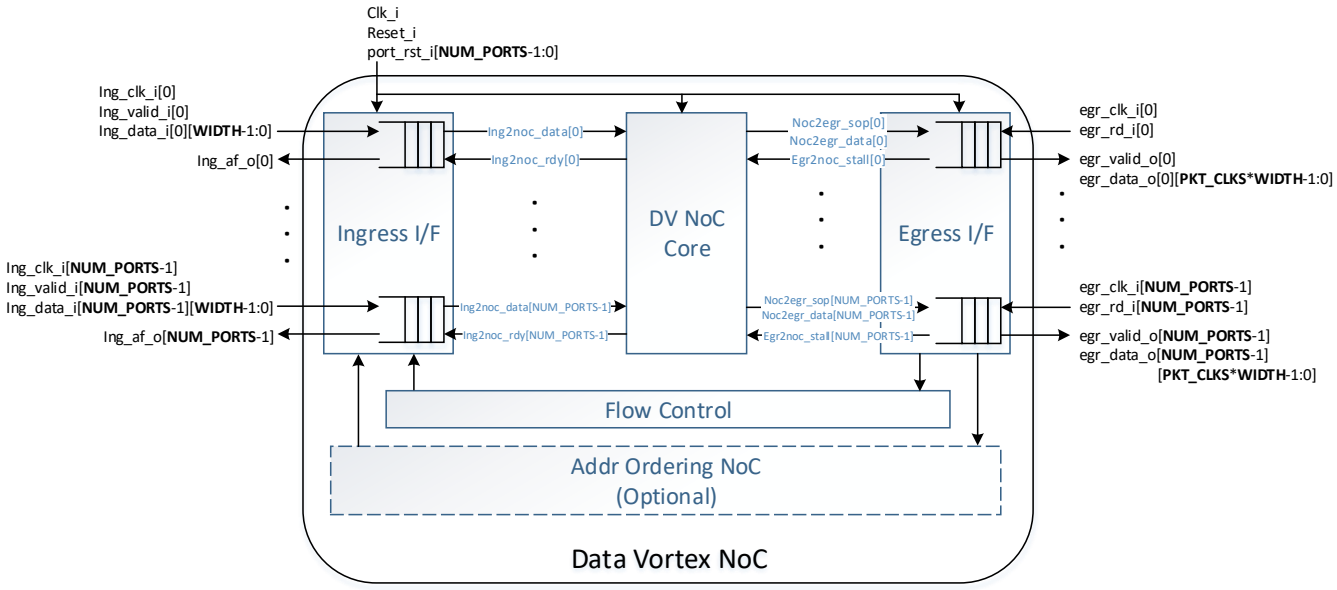
The DV NoC™ is a configurable lite weight, low latency, fine grain network on a chip that supports high radix applications. The DV NoC™ enables a multitude of blocks to communicate with each other over a fine grain network.

FEATURES

- Configurable number of ports (radix)
- Configurable number of bits per packet
- Configurable number of clocks per packet
- Configurable number of angles (size) of switch
- Supports ordered and unordered traffic

BLOCK DIAGRAM

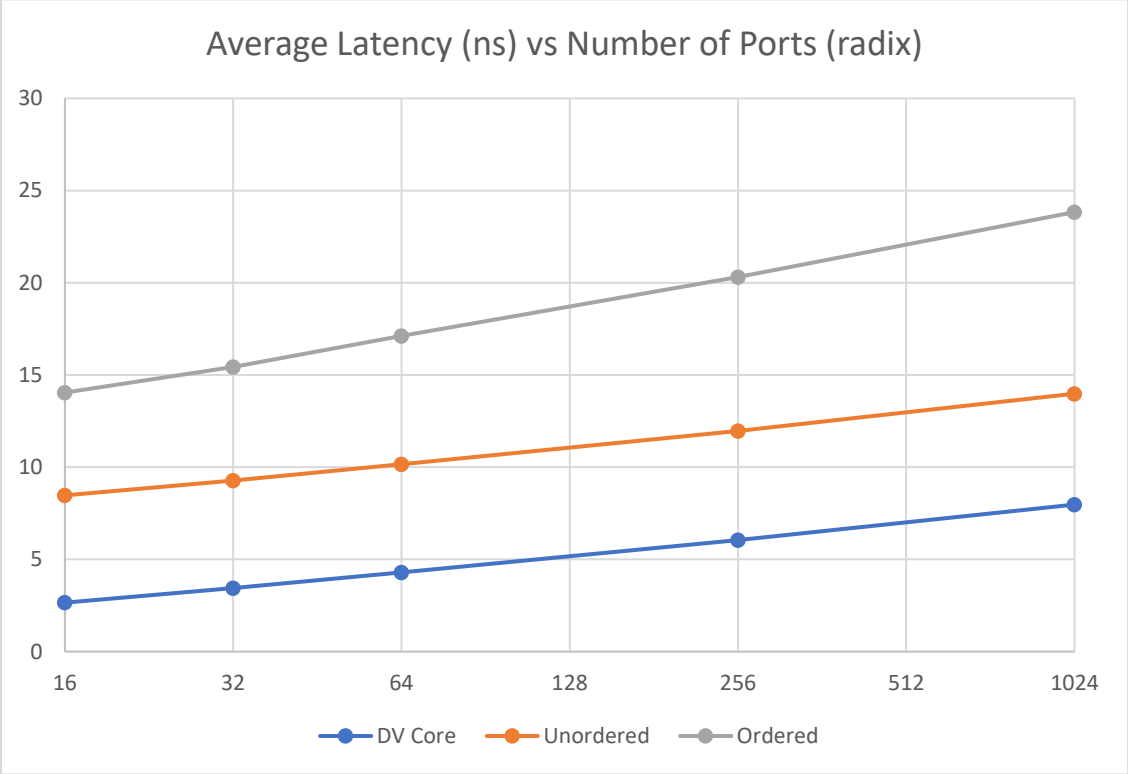
The DV NoC™ contains a wrapper that includes ingress, egress, and flow control blocks to simplify interconnecting to the DV NoC™ Core. A user may choose to implement their own ingress, egress, and flow control blocks and directly connect to the DV NoC™ Core block.



SIMULATIONS

The DV NoC™ average latency simulation results are depicted below. The input stimulus is one million total packets. Each packet consists of a random output port address and a random ordering selection (ordered or unordered packet type). Packets enter all ports at 100% input line rate. The results depict multiple simulations where the radix, NOC_PORTS, parameter was swept from 16 to 1024. The remaining parameters and clocks were configured as:

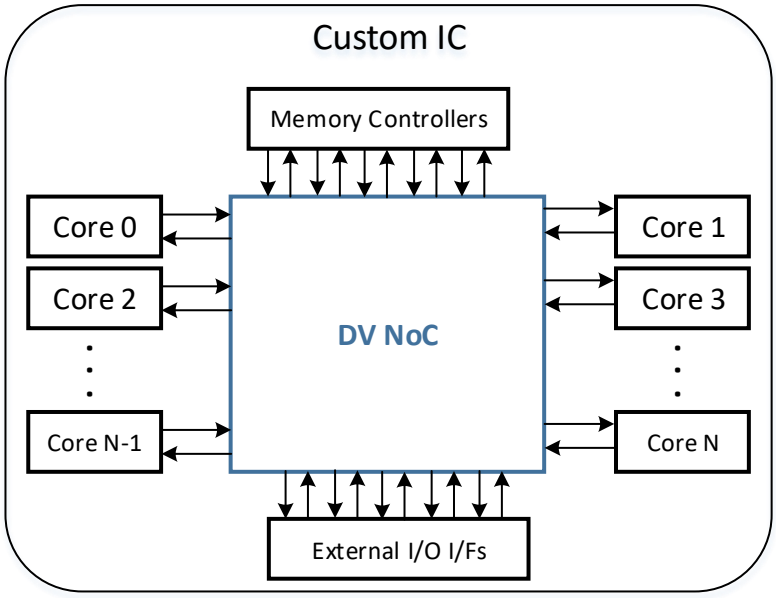
Name	Setting
NOC_PORTS	Swept
WIDTH	256
PKT_CLKS	2
COLUMNS	2
NOC_IN_ANGLES	2
Ing_clk_i & egr_clk_i	2.0 GHz
Clk_i	2.4 GHz



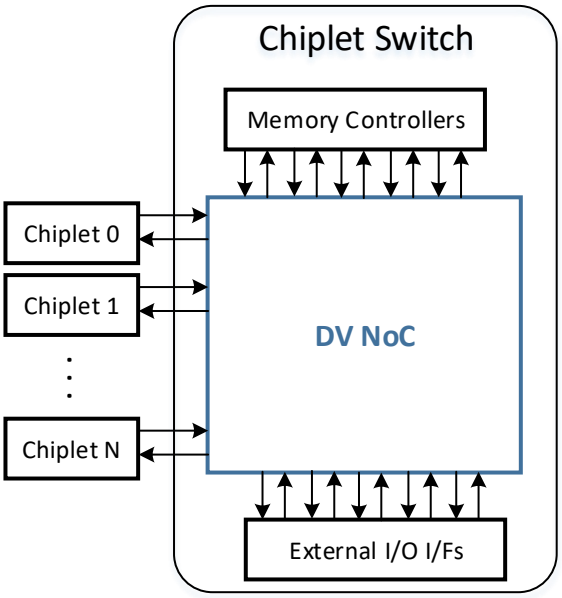
USE CASE EXAMPLES

The DV NoC™ can be used in a number of use cases such as:

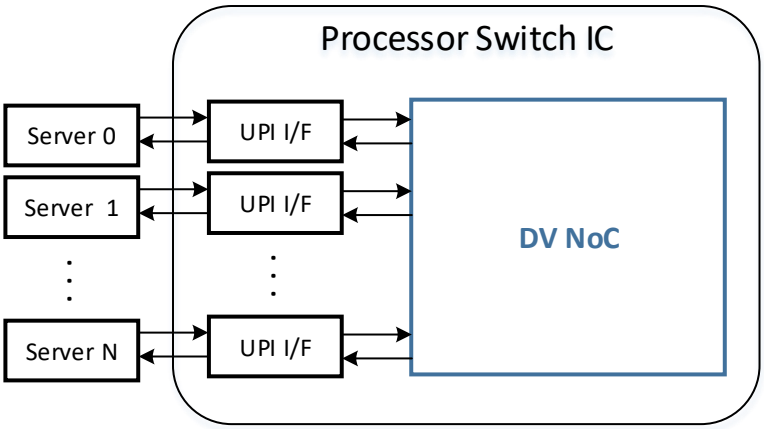
- Interconnecting cores, memory controllers, custom user blocks, etc. within an IC



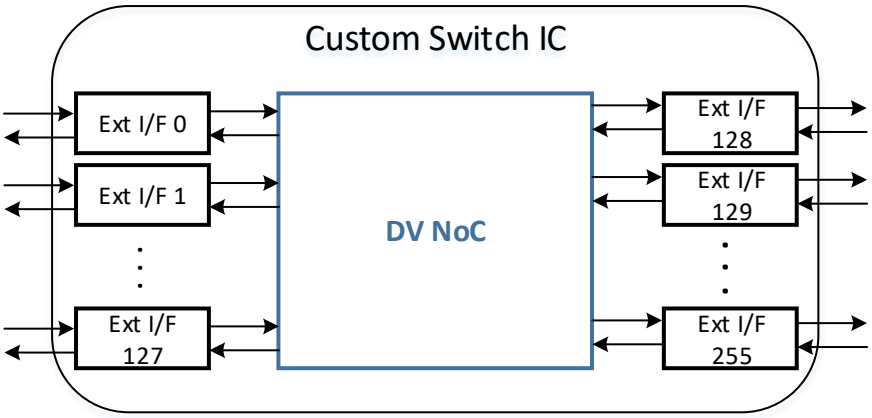
- Enabling a low latency chiplet switch IC



- Enabling a scalable low latency memory semantic processor switch IC, supporting large scalable unified memory systems.



- Enabling a memory semantic network switch chip. The custom switch enables large scalable multilevel networks supporting shared memory and/or disaggregation.



I/O SIGNALS

The DV NoC™ with wrapper I/Os are depicted in the block diagram in black and are described in Table 1.

Port Name	Description
Clk_i	DV NoC Core clock which should be >= to the ing_clk_i rates.
Reset_i	Global reset
Port_rst_i[NOC_PORTS-1:0]	Reset for each port
Ing_clk_i[NOC _PORTS-1:0]	Ingress clock for each port
Ing_valid_i[NOC _PORTS-1:0]	The valid bit must be set high on the first clock when a new packet enters the ingress block.
Ing_data_i[NOC _PORTS-1:0] [WIDTH-1:0]	Input data bus per port. The width of the bus can be set to the desired number of bits per clock tick. The PKT_CLKS parameter defines the number of clock ticks per packet so the total number of bits per packet = PKT_CLKS * WIDTH.
Ing_af_o[NOC _PORTS-1:0]	The port's ingress FIFO is almost full so only send in 1 more packet when ing_af_o goes high.
Egr_clk_i[NOC _PORTS-1:0]	Egress clock for each port
egr_rd_i[NOC _PORTS-1:0]	When egr_rd_i is high, packets will continue to pop out of the egr_data_o port. To stall egress traffic, the user must set egr_rd_i.
egr_valid_o[NOC _PORTS-1:0]	The port's egr_data_o bus contains a valid packet when egr_valid_o is high.
Egr_data_o[NOC _PORTS-1:0] [PKT_CLKS*WIDTH-1:0]	Output data bus per port. The width of the bus is a complete packet. Egr_data_o is valid when the respective egr_valid_o signal is high. The data is popped off the bus when both egr_rd_i and egr_valid_o are high; otherwise the packet is maintained on the bus.

Table 1: DV Wrapper I/O Signals

The DV Core may be used without the wrapper. If using the DV core stand alone, the utilized I/Os are depicted in the block diagram in blue and are described in Table 2.

Port Name	Description
Clk_i	DV NoC Core clock. All I/Os are synchronous to this clock with the exception of reset_i.
Reset_i	Global reset
Ing_rdy_o[PORTS-1:0]	When high, the first word of the packet can be sent into the NoC Core on ing_data_i. Once the first word is sent, the entire packet must be sent in the subsequent clocks with no idle data within those clocks. Ing_rdy_o is a periodic signal so it does not stay high on consecutive clocks.
Ing_data_i[PORTS-1:0] [NOC_IN_ANGLES-1:0] [WIDTH-1:0]	Input data bus per port. The width of the bus can be set to the desired number of bits per clock tick. The PKT_CLKS parameter defines the number of clock ticks per packet so the total number of bits per packet = PKT_CLKS * WIDTH. The most significant bit of the first word of the packet is the valid signal. When the MSb is high and ing_rdy_o is high, a packet enters the DV NoC Core. The full packet must be sent on consecutive clock ticks.
Egr_stall_i[PORTS-1:0] [COLUMNS-1:0]	Setting egr_stall_i high will eventually halt traffic coming out of the respective egr_data_o bus. One packet may still be output after the egr_stall_i signals is set high.
Egr_sop_o[PORTS-1:0] [COLUMNS-1:0]	A port's egr_data_o bus contains the first word of a valid packet when egr_sop_o is high. The user must accept the first word along with the remaining words of the entire packet when egr_sop_o is high on the first packet word.

Egr_data_o[PORTS-1:0] [COLUMNS-1:0][WIDTH-1:0]	A ports Egr_data_o bus is valid for PKT_CLK ticks starting on the clock when egr_sop_o is high. Once the first word of a packet is valid, all remaining words of that packet will be output on consecutive clocks.

Table 2: DV Core I/O Signals

PARAMETERS

Verilog parameters that configure the DV NoC™ are depicted in Table 3.

Parameter Name	Description
NOC_PORTS	Number of ports on NoC. The NoC radix = NOC_PORTS.
WIDTH	Bus width of the ingress port. The egress port width is PKT_CLKS * WIDTH.
PKT_CLKS	Number of clock ticks for a single packet. The fixed packet size = PKT_CLKS * WIDTH.
COLUMNS	Number of angles in the DV NoC. Used to size the switch logic.
NOC_IN_ANGLES	Number of angles input data can enter into the DV NoC Core.

Table 3: DV NoC Parameters

The WIDTH, PKT_CLKS, and COLUMNS parameters can be utilized to adjust the DV NoC bandwidth and size.

PATENTS NOTICE

Technologies in this product brief are covered by PAT: US 9,634,862; US 9,954,797; US 10,630,607; US 2020/0195584 A1 (Pending), US 17/095,866 (Submitted), assigned to Interactic Holdings, LLC.

CONTACT INFORMATION

For more details on the DV NoC™, please email contact@datavortex.com.